What is Claimed is:

1. A method for fabricating a vertical nitride read-only memory (NROM) cell, comprising the steps of:

providing a substrate having at least one trench;

forming doping areas as bit lines in the substrate near its surface and the bottom of the trench;

forming bit line oxides over each of the doping areas;

forming a conformable insulating layer as gate dielectric on the sidewall of the trench and the surface of the bit line oxide; and

forming a conductive layer as a word line over the insulating layer and filling in the trench.

2. The method as claimed in claim 1, wherein the trench has a depth of about 1400~1600 Å.

3. The method as claimed in claim 1, wherein formation of the doping areas further comprises:

forming a spacer over the sidewall of the trench; and

performing ion implantation in the substrate using the spacer as a mask.

4. The method as claimed in claim 3, wherein the spacer is silicon nitride.

5. The method as claimed in claim 3, wherein the ion implantation is performed by phosphorus.

6. The method as claimed in claim 3, further removing the spacer before formation of the conformable insulating layer.

7. The method as claimed in claim 1, wherein the bit line oxides are formed by thermal oxidation.

8. The method as claimed in claim 1, wherein the bit line oxides have a thickness of about 500~700 Å.

9. The method as claimed in claim 1, wherein the insulating layer is an oxide-nitride-oxide layer.

10. The method as claimed in claim 1, wherein the conductive layer is polysilicon.